CLAIMS

1. A controller for a multiphase converter, comprising:

an error amplifier having an input for coupling to a feedback resistance and an output that generates an error signal based on an error voltage developed across said feedback resistance;

a gain resistor;

a current sense circuit that converts each of a plurality of sensed load currents into a corresponding one of a plurality of proportional voltages; and

a gain adjust amplifier circuit, having an input coupled to receive said plurality of proportional voltages and an output coupled to said gain resistor and said error amplifier input, that applies at least one gain adjust voltage to said gain resistor to develop a gain adjust current through said feedback resistance.

2. The controller of claim 1, wherein said current sense circuit comprises:

a plurality of sense resistors, each having a first end and a second end coupled to a corresponding one of a plurality of phase nodes of the converter;

a plurality of sense amplifiers, each having a first input coupled to said first end of a corresponding one of said plurality of sense resistors and a second input coupled to a first reference voltage;

a plurality of variable impedance devices, each coupled to an output and to said first input of a corresponding one of said plurality of sense amplifiers;

a plurality of current sense translation resistors, each coupled between a corresponding one of said plurality of variable impedance devices and a second reference voltage; and

a plurality of sample and hold circuits, each coupled to a corresponding one of said plurality of current sense translation resistors for providing a corresponding one of said plurality of proportional voltages.

3. The controller of claim 1, wherein said current sense circuit comprises:

a plurality of sense resistors, each having a first end and a second end coupled to a corresponding one of a plurality of phase nodes of the controller;

a switched sense amplifier circuit, comprising:

select logic coupled to said first end of each of said plurality of sense resistors;

a sense amplifier having a first input coupled to said select logic and a second input coupled to a first reference voltage;

a variable impedance device coupled to an output and to said first input of said sense amplifier; and

a current sense translation resistor coupled between a second reference voltage and said variable impedance device; and

a plurality of sample and hold circuits, each coupled to said current sense translation resistor for providing a corresponding one of said plurality of proportional voltages.

4. The controller of claim 1, wherein said gain adjust amplifier circuit comprises:

select logic that selects among said plurality of proportional voltages;

a gain adjust amplifier having a first input coupled to said select logic and a second input coupled to said gain resistor; and

a variable impedance device having a control input coupled to an output of said gain adjust amplifier, a first current terminal coupled to said gain resistor and a second current terminal coupled to said error amplifier input.

5. The controller of claim 1, wherein said variable impedance device comprises a P-channel field-effect transistor.

6. The controller of claim 1, wherein said gain adjust amplifier circuit comprises:

select logic that time multiplexes said plurality of proportional voltages; and

a gain amplifier that controls a variable impedance device to generate said gain adjust current through said gain resistor by applying a selected proportional voltage to said gain resistor.

7. The controller of claim 1, wherein said gain adjust amplifier circuit further comprises an averaging circuit that averages said plurality of proportional voltages to provide said at least one gain adjust voltage.

8. An integrated circuit (IC) incorporating a multiphase converter controller, comprising:

a feedback pin for coupling a feedback resistor;

a gain pin for coupling a gain resistor;

an error amplifier having a first input coupled to said feedback pin and an output that provides an error signal based on a voltage across said feedback resistor;

pulse-width modulation (PWM) logic, coupled to said output of said error amplifier, that develops a plurality of PWM signals based on said error signal;

a plurality of drivers, each receiving a corresponding one of said plurality of PWM signals and each having a corresponding one of a plurality of phase nodes;

a plurality of sense resistors, each having a first end coupled to a corresponding one of said plurality of phase nodes;

a current sense circuit, coupled to a second end of each of said plurality of sense resistors, that converts a current developed through each sense resistor into a corresponding one of a plurality of proportional load voltages; and

a gain adjust current generator having an input receiving said plurality of proportional load voltages and a current-controlled output for developing a gain adjust current through said gain resistor by maintaining a selected proportional load voltage on said gain pin and applying said gain adjust current through said feedback resistor via said feedback pin.

9. The IC of claim 8, wherein said current sense circuit comprises:

a plurality of sense amplifiers, each having a first input coupled to said second end of a corresponding one of said plurality of sense resistors and a second input coupled to a first DC voltage level;

a plurality of variable impedance devices, each coupled to an output and to said first input of a corresponding one of said plurality of sense amplifiers;

a plurality of current sense translation resistors, each coupled between a corresponding one of said plurality of variable impedance devices and a second DC voltage level; and

a plurality of sample and hold circuits, each coupled to a corresponding one of said plurality of current sense translation resistors for providing a corresponding one of said plurality of proportional load voltages.

10. The IC of claim 8, wherein said current sense circuit comprises:

select logic coupled to said second end of each of said plurality of sense resistors;

a sense amplifier having a first input coupled to said select logic and a second input coupled to a first DC voltage level;

a variable impedance device coupled to an output and to said first input of said sense amplifier;

a current sense translation resistor coupled between a second DC voltage level and said variable impedance device; and

a plurality of sample and hold circuits, each having an input coupled to said current sense translation resistor and an output for providing a corresponding one of said plurality of proportional load voltages.

11. The IC of claim 8, wherein said gain adjust current generator comprises:

select logic that selects from among said plurality of proportional load voltages;

a gain adjust amplifier having a first input coupled to said select logic and a second input coupled to said gain pin; and

a variable impedance device having a control input coupled to an output of said gain adjust amplifier, a first current terminal coupled to said gain pin and a second current terminal coupled to said feedback pin.

12. The IC of claim 11, wherein said select logic comprises a multiplexer that provides each of said plurality of proportional load voltages to said gain adjust amplifier one at a time.

13. The IC of claim 11, further comprising an averaging circuit coupled to said select logic that averages said plurality of proportional load voltages and that provides an average voltage to said gain adjust amplifier.

14. The IC of claim 11, wherein said variable impedance device comprises a P-channel field-effect transistor having a gate coupled to said output of said gain adjust amplifier and a drain and source coupled between said gain and feedback pins.

15. A method of adjusting gain of a multiphase power converter comprising:

generating a plurality of currents, each representative of a corresponding load current sensed at a corresponding one of a plurality of phase nodes;

applying each representative current through at least one current sense translation resistor;

sampling voltage developed across the at least one current sense translation resistor and providing a plurality of sensed voltages each representative of a corresponding load current;

selecting from among the plurality of sensed voltages to provide at least one gain adjust voltage;

applying the at least one gain adjust voltage to a gain resistor to develop a gain adjust current through the gain resistor; and

applying the gain adjust current through a feedback resistor to adjust gain.

16. The method of claim 15, wherein said generating a plurality of currents comprises sensing current through a plurality of sense resistors coupled to the corresponding plurality of phase nodes with at least one virtual ground amplifier that controls at least one variable impedance device.

17. The method of claim 16, wherein said applying each representative current comprises coupling each of the at least one current sense translation resistor in series with a corresponding one of the at least one variable impedance device.

18. The method of claim 15, wherein said selecting from among the plurality of sensed voltages comprises time multiplexing.

19. The method of claim 15, wherein said selecting from among the plurality of sensed voltages comprises averaging the plurality of sensed voltages and providing an average voltage.

20. The method of claim 15, wherein said applying the at least one gain adjust voltage to a gain resistor to develop a gain adjust current through the gain resistor and said applying the gain adjust current through a feedback resistor to adjust gain comprises applying the at least one gain adjust voltage to the gain resistor through a negative feedback path of an amplifier having an output controlling a variable gain device coupled in series with the gain and feedback resistors.